

DESCRIPTION

Sanland's AL34 is an economical, easy-to-use GaAs MMIC Low Noise Amplifier (LNA). The LNA has low noise and high linearity achieved through the use of 0.5um GaAs Enhancement-mode pHEMT process. It is housed in a miniature 2.0 x 2.0 x 0.75mm³ 8-pin Quad-Flat-Non-Lead (QFN) package. It is designed for optimum use from 1.5GHz up to 2.6GHz. The compact footprint and low profile coupled with low noise, high gain and high linearity make the AL34 an ideal choice as a low noise amplifier for cellular infrastructure for GSM and CDMA.

KEY FEATURES

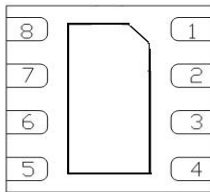
- 0.5dB noise figure at 1900MHz
- 35dBm Output IP3 at 1900MHz
- Optimum use from 1.5GHz up to 2.6GHz
- Small package size: 2.0 x 2.0 x 0.75mm³
- Single 5V Supply
- ESD 250V HBM
- MSL: Level 1
- Share the same package and pin configuration with AL33 use from 0.4GHz to 1.5GHz



Major Applications

- LNA for cellular infrastructure and other ultra low noise application.

Pin Assignment



QFN2X2-8L

Pin Details

Pin Number	Name	Description
1	Vbias	Gate Voltage
2	RF in	RF Input
3,4,5,6,8	N/C	Good RF practice require N/C pins to be earthed
7	RF OUT	RF output.
Exposed PAD	GND	Multiple vias should be employed to minimize inductance and thermal resistance

Electrical Characteristics for Application

(VDD =+5V; unless otherwise noted.)

Parameter	Specification			Units	Notes	
	Min	Typ.	Max			
Freq	1.5		2.6	GHz		
Gain	17.0	18.4	20.0	dB	1900MHz	
		17.0		dB	2100MHz	
		15.5		dB	2400MHz	
		14.7		dB	2600MHz	
P-1dB	19	21		dB	1900MHz	
		21		dB	2100MHz	
		21		dB	2400MHz	
		21		dB	2600MHz	
OIP3	33	36		dB	1900MHz	
	33	36		dB	2100MHz	
	32	34.5		dB	2400MHz	
	31	33.5		dB	2600MHz	
Input return loss		-20	-16	dB	1900MHz	
		-18		-15	dB	2100MHz
		-17			dB	2400MHz
		-17			dB	2600MHz
Output return loss		-10		dB	1800~2600MHz	
NF		0.5	0.69	dB	1900MHz	
		0.6	0.8	dB	2100MHz	
		0.75	0.9	dB	2400MHz	
		0.9	1.0	dB	2600MHz	
Reverse Isolation		-29			1800~2600MHz	
VDD		5.0	5.5	V		
IDD	40	50	70	mA		
Test Conditions : VDD=5V, IDD=55mA Typ. OIP3 Tone Spacing=1MHz, Pout per ton=+5 dBm TL=25°C, ZS=ZL=50 Ohms						

Absolute Maximum Ratings

Parameter	Rating	Unit
DC Power Supply	+5.5	V
DC Supply Current at VDD	90	mA
RF Input Power	+20	dBm
Max. Operating Dissipated Power	0.5	W
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-65 to +150	°C
Max. Junction Temp. (TJ)	+150	°C
R _{TH}	68	°C/W
Operation beyond any one of these limits may cause permanent damage.		

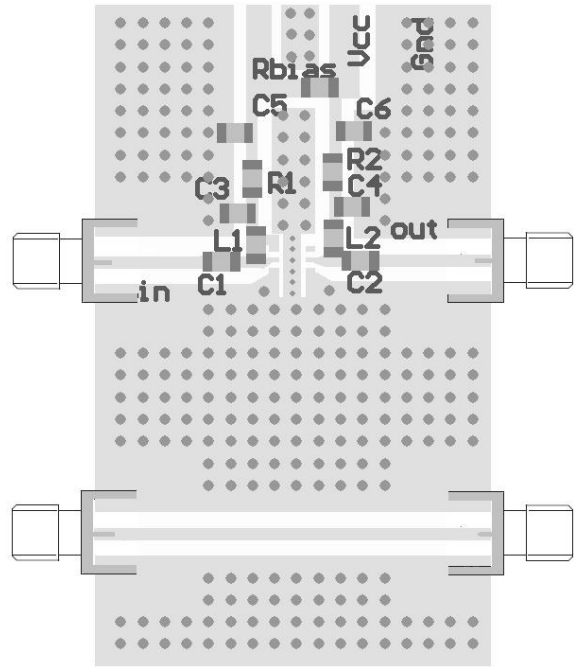
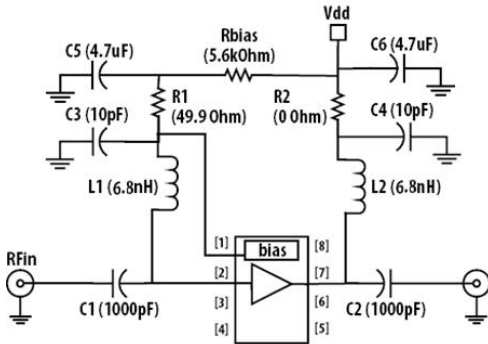
Important Note:

The information provided in this datasheet is deemed to be accurate and reliable only at present time. Sanland Technology Corp. reserves the right to make any changes to the specifications in this datasheet without prior notice.



Caution: ESD Sensitive
 Appropriate precaution in handling, packaging
 And testing devices must be observed.

Application Circuit



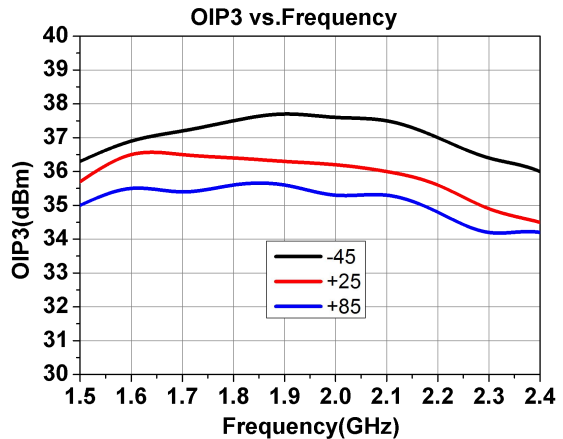
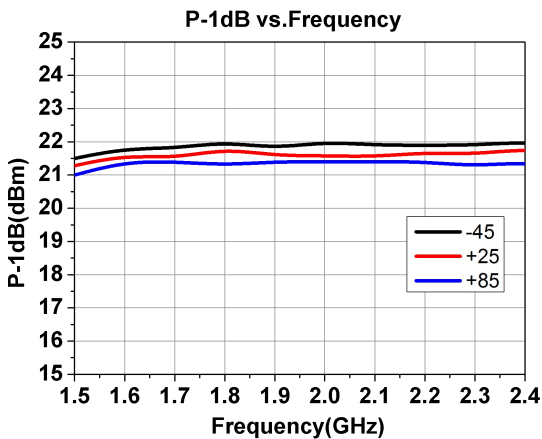
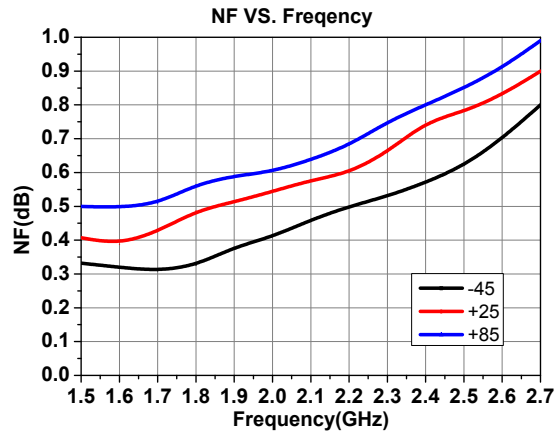
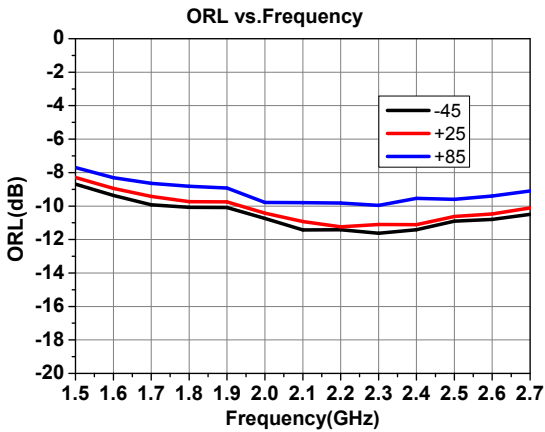
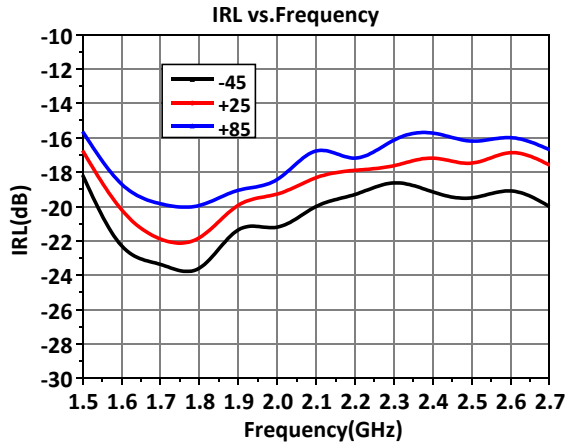
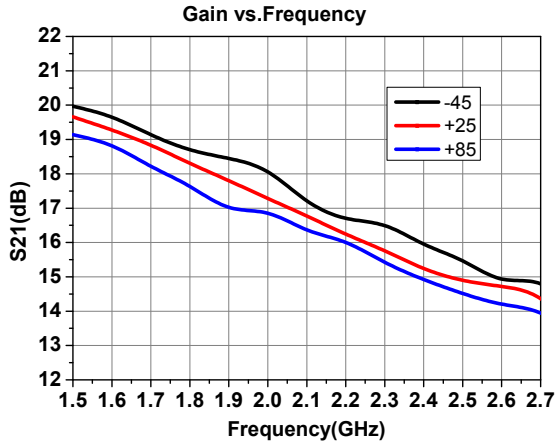
Part	Size	Value
C1, C2	0402	1000pF (Murata)
L1	0402	6.8 nH (CoilCraft)
L2	0402	6.8 nH (CoilCraft)
C3, C4	0402	10pF (Murata)
C5, C6	0805	4.7uF (Murata)
R1	0402	49.9 Ohm (Rohm)
R2	0402	0 Ohm (Rohm)
Rbias	0402	5.6 kohm (Rohm)

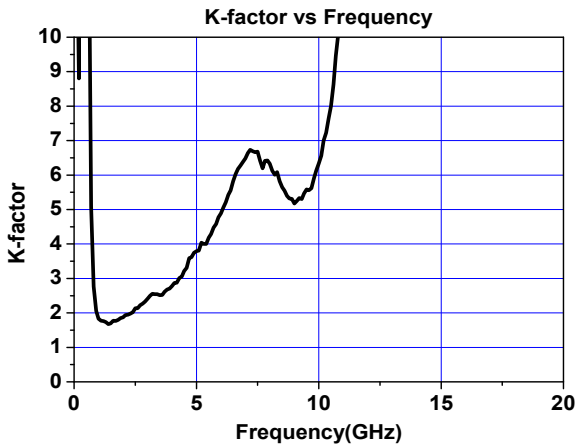
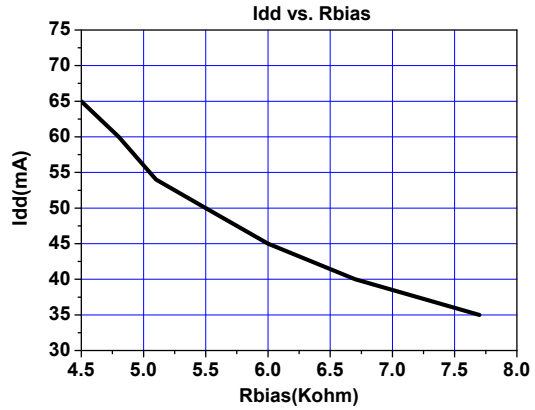
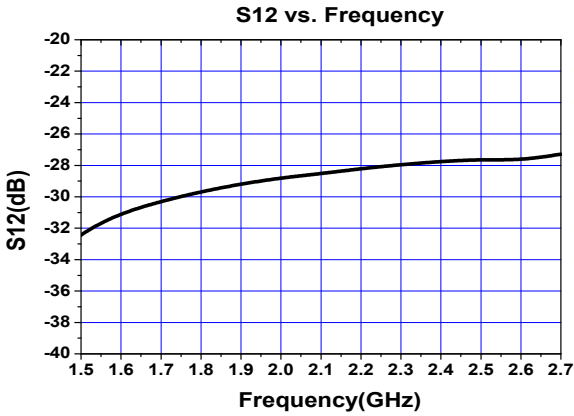
Note:

C1, C2 are DC Blocking capacitors; L1 input match for NF;
 L2 output match for OIP3; C3, C4, C6 are bypass capacitors; R1 is stabilizing resistor;
 Rbias is the biasing resistor (5.6kOhm ref.) ; C5 are not use for this product

Performance Plots With Demo Board

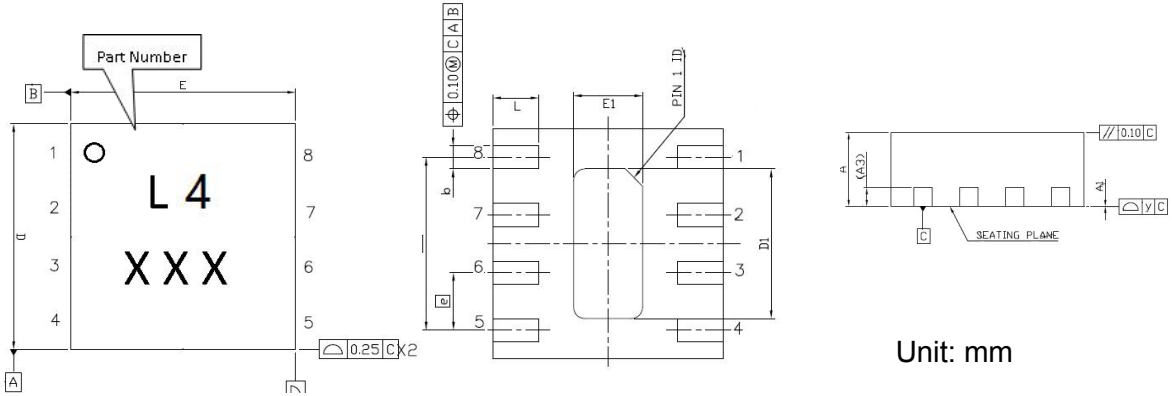
Test conditions: $V_D=5V$, $R_{bias}=5.6k\Omega$, $I_d=50mA$, $Z_S=Z_L=50\ \Omega$. OIP3 test conditions: OIP3 Tone Spacing=1MHz, Pout per tone=5 dBm





NOTE: The K-Factor tested using demo board with good RF/DC grounding. Inductance to grounding will reduce K-Factor.

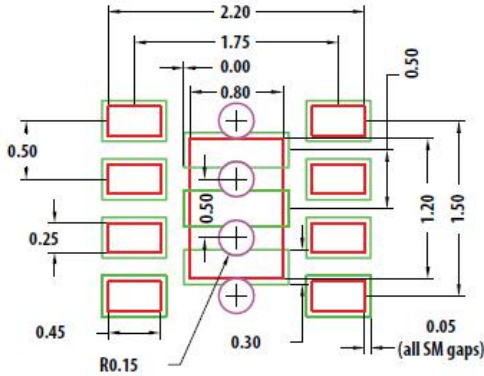
Package Outline



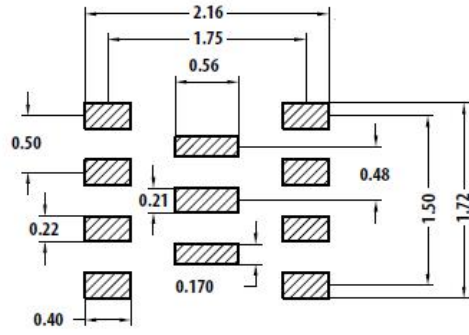
SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	27.6	29.5	31.5
A1	0.00	0.02	0.05	0	0.8	2
A3	0.20 REF			8 REF		
b	0.15	0.20	0.25	6	8	10
D	2.00 BSC			79 BSC		
D1	1.25	1.30	1.35	49.2	51.2	53.2
E	2.00 BSC			79 BSC		
E1	0.55	0.60	0.65	21.6	23.6	25.6
\overline{e}	0.50 BSC			19.7 BSC		
$\overline{e1}$	1.50 BSC			59 BSC		
L	0.30	0.40	0.50	11.8	15.7	19.7
y			0.08			3

Note: This package is lead-free, RoHS-compliant, and green. The plating material on the pins is annealed matte tin over copper. It is compatible with both lead-free(maximum 260°C reflow temperature) and leaded (maximum) 245°C reflow temperature).

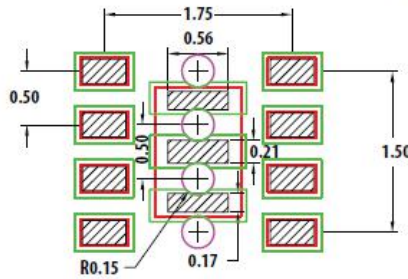
Suggested PCB Layout



Land Pattern



Stencil Opening



NOTES:

1. Dimensions are in millimeter.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under backside paddle for proper RF/DC grounding and thermal dissipation. Via holes could reduce lead inductance as close to ground as possible.
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.